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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,039	04/20/2004	Brian C. Taggart	042390.P18809	7420

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 09/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/829,039	TAGGART ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see remarks, filed 7/17/06, with respect to the rejection(s) of claim(s) 1-6 and 8-14 under 102 rejection have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Katoh (US 6,555,907).

Drawings

2. The formal drawings filed on 4/20/04 have been approved by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 4-6 and 8-14 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Katoh (US 6,555,907).

With respect to Claim 1, Katoh teaches at least a first die 12 having an integrated circuit formed therein and at least one redistribution conductor 30 (i.e. wiring layers) including a pair of contacts 28a,18 or 28b,28c on the die 12. At least one pair of redistribution wire bonding wires 48, each redistribution wire bonding 48 having a respective die portion, the die portions of the respective bonding wires 48 being

electrically attached to the respective contacts 28a,18 or 28b,28c of the redistribution conductor 30 (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 2, Katoh teaches a plurality of redistribution conductors 30, each including a respective pair of contacts on the die. A plurality of pairs of redistribution wire bonding wires, each redistribution wire bonding wire having a respective die portion, the die portions of the respective wire bonding wires being electrically attached to the respective contacts of the redistribution conductors so as to connect a respective one of the pairs of redistribution wire bonding wires through a respective redistribution conductor to one another (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claims 4 and 6, Katoh teaches at least a first component 40 (i.e. substrate) other than the die. At least a first terminal 44 on the first component a first of the redistribution wires of the pair having a component portion attached to the terminal, wherein the terminals is outside an area of the die (see col. 7 lines 30-67 and col. 8 lines 1-14; Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 5, Katoh teaches at least a second terminal 44 on the first component, the other redistribution wire of the pair having a component portion attached to the terminal (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 8, Katoh teaches at least a third contact on the die, a second of the redistribution wire bonding wires of the pair having apportion attached to the third contact (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 9, Katoh teaches a substrate 40, a microelectronic die 12 having an integrated circuit formed therein and mounted to the substrate 40. A pair of redistribution terminals 44 is on the substrate 40. A redistribution conductor 30 interconnecting the redistribution terminals, the redistribution conductor 30 including a redistribution contact 28a,18 or 28b,28c on the die 12 and a bonding wire 48 having first and second portions electrically attached to one of the redistribution terminals and to the redistribution contact 28a,18 or 28b,28c, respectively (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to claim 10, Katoh teaches a plurality of pairs of redistribution terminals on the substrate and a plurality of redistribution conductors, wherein each interconnecting the redistribution terminals of a respective pair. Each redistribution conductor including a redistribution contact on the die and a wire bonding wire having first and second portions electrically attached to one of the redistribution terminals and to one of the redistribution contacts, respectively (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 11, Katoh teaches conductor includes a pair of redistribution contacts on the die and a pair of redistribution wire bonding wires, each redistribution wire bonding wire having a respective first portion electrically attached to a respective one of the redistribution terminals of the pair and a respective redistribution contact of the pair (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 12, Katoh teaches a substrate 40, a microelectronic die 12, having an integrated circuit formed therein and mounted to the substrate 40. A plurality of functional terminals is on the substrate 40. A plurality of functional contacts 38 on the

die 20, each being connected to the integrated circuit. A plurality of functional wire bonding wires 28, each having a first portion attached to a respective functional terminal and a second portion attached to a respective functional contact 28a,18 or 28b,28c . A pair of redistribution terminals 44 on the substrate 40 and a redistribution conductor 30, interconnecting the redistribution terminals, the redistribution conductor 30 including a redistribution contact 28a,18 or 28b,28c on the die 12 and a wire bonding wire 48 having first and second portions electrically attached to one of the redistribution terminals and to the redistribution contact 28a,18 or 28b,28c, respectively (see Figs. Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 13, Katoh teaches wherein the redistribution conductor is not physically connected to the integrated circuit between the redistribution contacts (see Figs. 1, 5, 10, 12, 15, 17, and 20).

With respect to Claim 14, Katoh teaches wherein the redistribution conductor includes a pair of redistribution contacts on the die and a pair of redistribution wire bonding wires, each redistribution wire bonding wire having a respective first portion attached to a respective one of the redistribution terminals of the pair and a respective redistribution contact of the pair (see Figs. 1, 5, 10, 12, 15, 17, and 20).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Katoh (US 6,555,907) as applied to claim 1 above, and further in view of Li et al. (US 5,838,072).

With respect to Claim 3, Katoh discloses the claimed invention except for a wire between contacts on a die. However, Li discloses a wire 35 or 45b between contacts 32b, 34 or 42b, 44b on a die 41 (see Fig. 4). Thus, Katoh and Li have substantially the same environment of a chip wire bonded to an external element. Therefore, one skilled in the art would readily recognize incorporating a wire between contacts of Katoh, since the wire would reduce the space taken on the chip by power buses and reduction in the voltage drop across the chip as taught by Li.

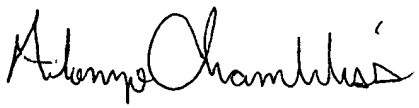
The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

7. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.



Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/September 23, 2006